## General Description

TW105N03 use advanced VD MOST technology to provide low RDS(ON), low gate charge, fast switching

This device is specially designed to get better ruggedness and suitable to use in

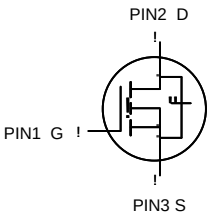
## Features

Low RDS(on) & FOM

Extremely low switching loss

Excellent stability and uniformity or Invertors

TO-252




## Applications

Consumer electronic power supply Motor control

Synchronous-rectification Isolated DC

Synchronous-rectification applications

## General Features

$V_{DS}$ = 30V $I_D$ =105 A

$R_{DS(ON)}$ < 5mΩ @ $V_{GS}$=10V

$R_{DS(ON)}$ < 7.5mΩ @ $V_{GS}$=4.5V

**Absolute Maximum Ratings** ($T_C$=25℃ unless otherwise specified)

| Symbol | Parameter | | Max. | Units |
|---|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | | 30 | V |
| $V_{GSS}$ | Gate-Source Voltage | | ±20 | V |
| $I_D$ | Continuous Drain Current | $T_C$ = 25℃ | 105 | A |
| | | $T_C$ = 100℃ | 58 | A |
| $I_{DM}$ | Pulsed Drain Current note1 | | 360 | A |
| $E_{AS}$ | Single Pulsed Avalanche Energy note2 | | 250 | mJ |
| $P_D$ | Power Dissipation | $T_C$ = 25℃ | 90 | W |
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case | | 1.67 | ℃/W |
| $T_J$, $T_{STG}$ | Operating and Storage Temperature Range | | -55 to +175 | ℃ |

**Electrical Characteristics** ($T_C$=25℃ unless otherwise specified)

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$=0V,$I_D$=250μA | 30 | - | - | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ =30V, $V_{GS}$ = 0V, | - | - | 1.0 | μA |
| $I_{GSS}$ | Gate to Body Leakage Current | $V_{DS}$ =0V,$V_{GS}$ = ±20V | - | - | ±100 | nA |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$= $V_{GS}$, $I_D$=250μA | 1.0 | 1.5 | 2.5 | V |
| $R_{DS(on)}$ | Static Drain-Source on-Resistance note3 | $V_{GS}$ =10V, $I_D$ =20A | - | 3.6 | 5 | mΩ |
| | | $V_{GS}$ =4.5V, $I_D$ =15A | - | 5 | 7.5 | |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$=5V, $I_D$=15A | - | 28 | - | S |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ =15V, $V_{GS}$ =0V, f = 1.0MHz | - | 1950 | - | pF |
| $C_{oss}$ | Output Capacitance | | - | 320 | - | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | - | 240 | - | pF |
| $Q_g$ | Total Gate Charge | $V_{DS}$ =25V, $I_D$=20A, $V_{GS}$ =10V | - | 42 | - | nC |
| $Q_{gs}$ | Gate-Source Charge | | - | 4 | - | nC |
| $Q_{gd}$ | Gate-Drain(“Miller”) Charge | | - | 14 | - | nC |
| $t_{d(on)}$ | Turn-on Delay Time | $V_{DS}$=15V, $R_l$=0.75Ω, $R_{GEN}$=3Ω, $V_{GS}$=10V | - | 13 | - | ns |
| $t_r$ | Turn-on Rise Time | | - | 36 | - | ns |
| $t_{d(off)}$ | Turn-off Delay Time | | - | 43 | - | ns |
| $t_f$ | Turn-off Fall Time | | - | 16 | - | ns |
| $I_S$ | Maximum Continuous Drain to Source Diode Forward Current | | - | - | 90 | A |
| $I_{SM}$ | Maximum Pulsed Drain to Source Diode Forward Current | | - | - | 360 | A |
| $V_{SD}$ | Drain to Source Diode Forward Voltage | $V_{GS}$ = 0V, $I_S$=30A | - | - | 1.2 | V |
| trr | Body Diode Reverse Recovery Time | $I_F$=20A,dI/dt=100A/μs | - | 16 | - | ns |
| Qrr | Body Diode Reverse Recovery Charge | | - | 5 | - | nC |

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. EAS condition: $T_J$=25℃,VDD=30V,VG=10V,L=0.5mH， RG=25 Ω

**Figure1:** Output Characteristics

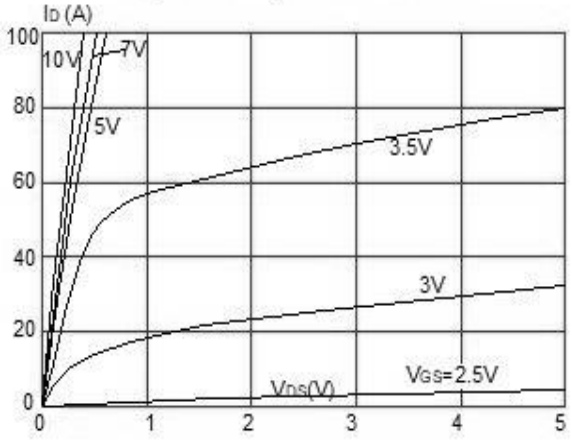



**Figure 2:** Typical Transfer Characteristics

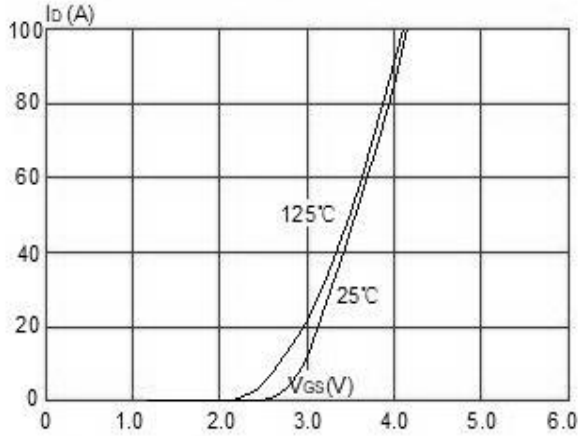



**Figure 3:** On-resistance vs. Drain Current

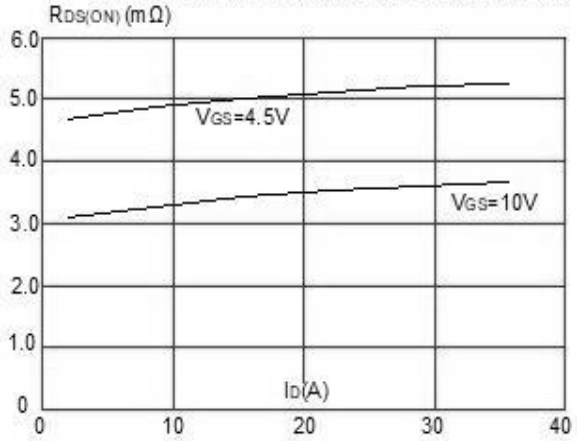



**Figure 4**: Body Diode Characteristics

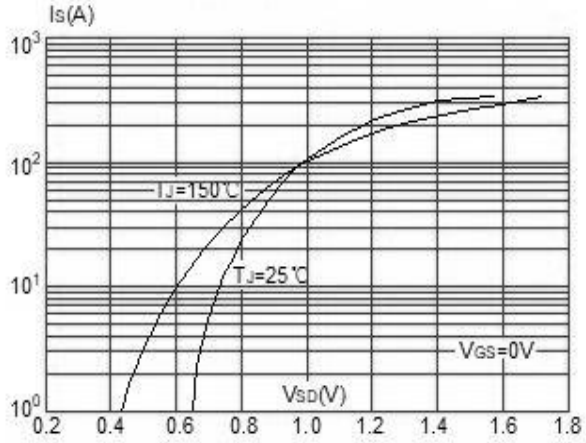



**Figure 5:** Gate Charge Characteristics

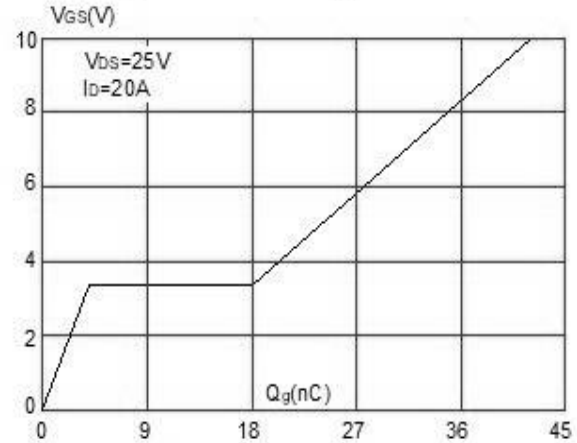



**Figure 6:** Capacitance Characteristics

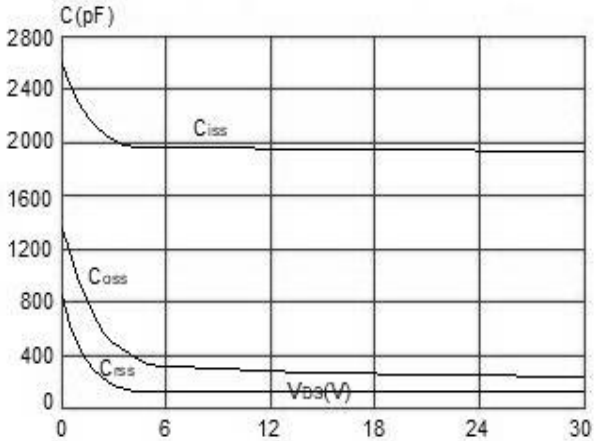


**Figure 7:** Normalized Breakdown Voltage vs. Junction Temperature

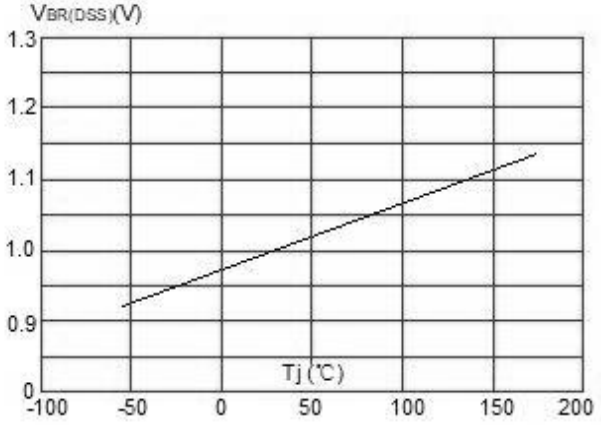



**Figure 8:** Normalized on Resistance vs. Junction Temperature

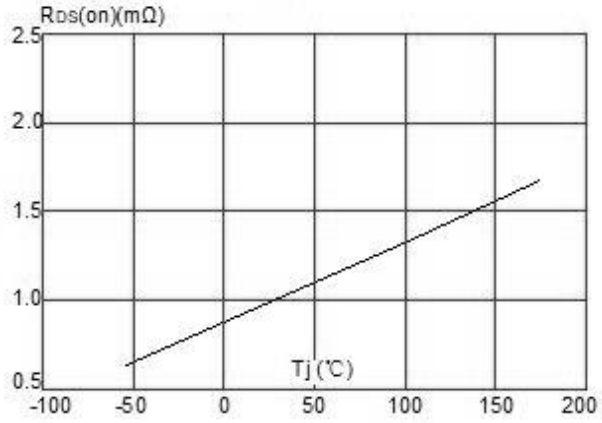



**Figure 9:** Maximum Safe Operating Area

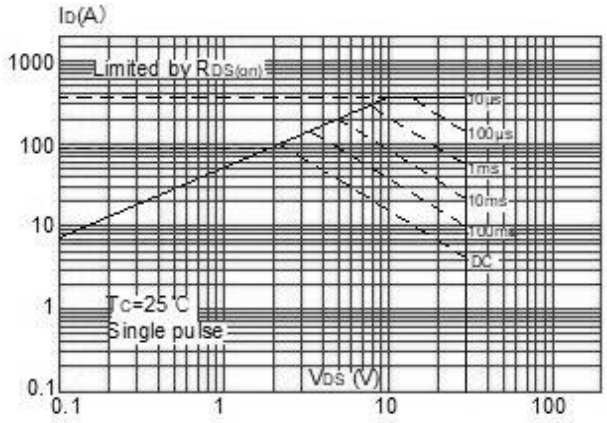



**Figure 10:** Maximum Continuous Drain Current vs. Case Temperature

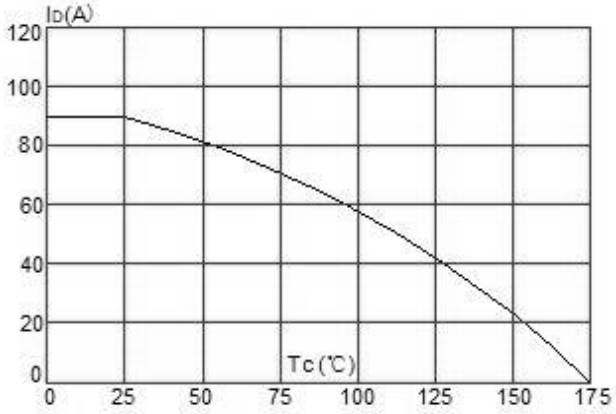
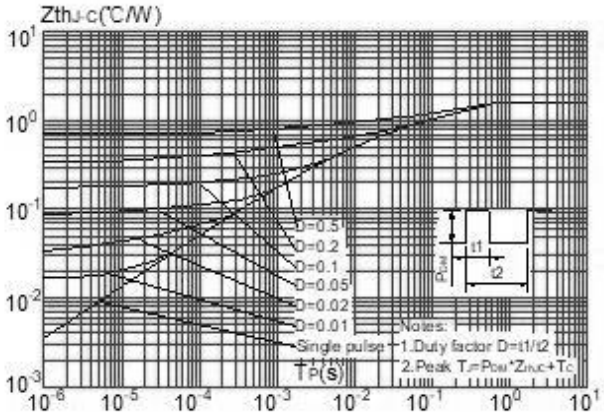



**Figure.11:** Maximum Effective Transient Thermal Impedance, Junction-to-Case (TO-252)



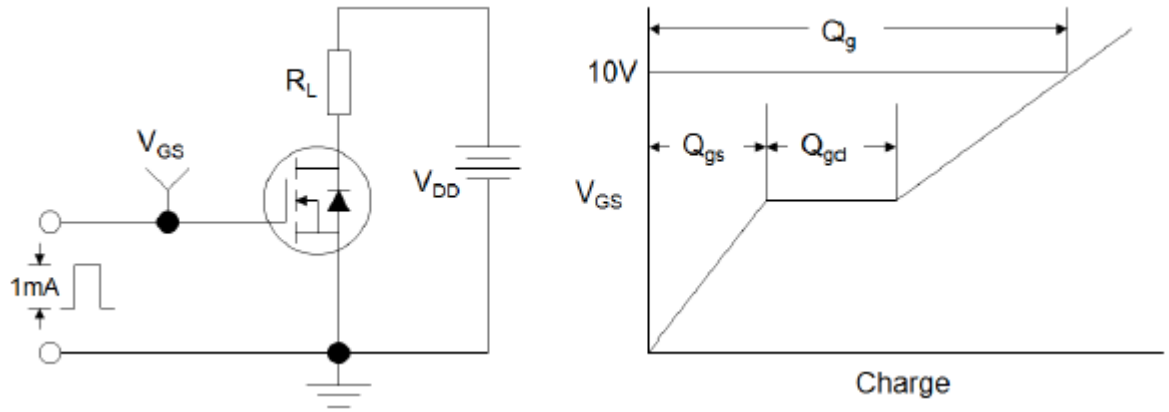



**Figure1:Gate Charge Test Circuit & Waveform**

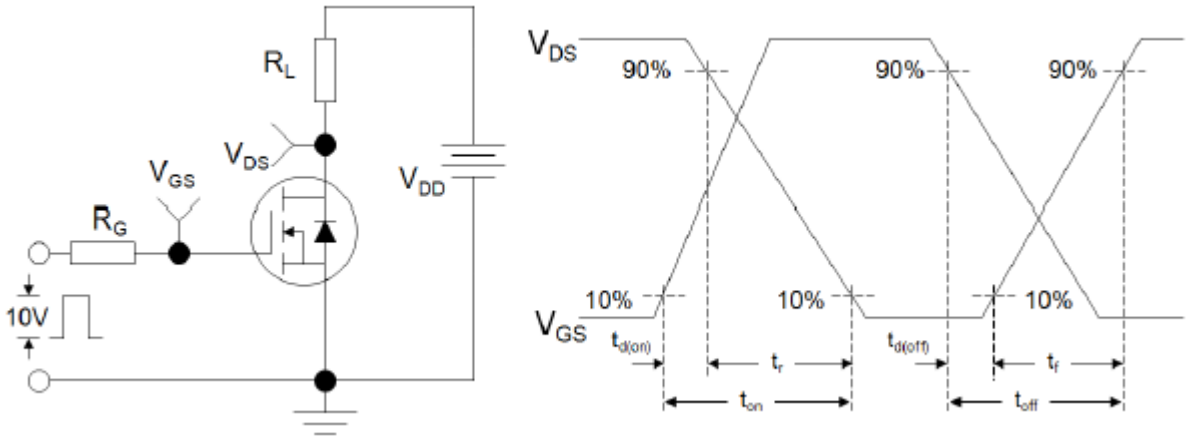



**Figure 2: Resistive Switching Test Circuit & Waveforms**

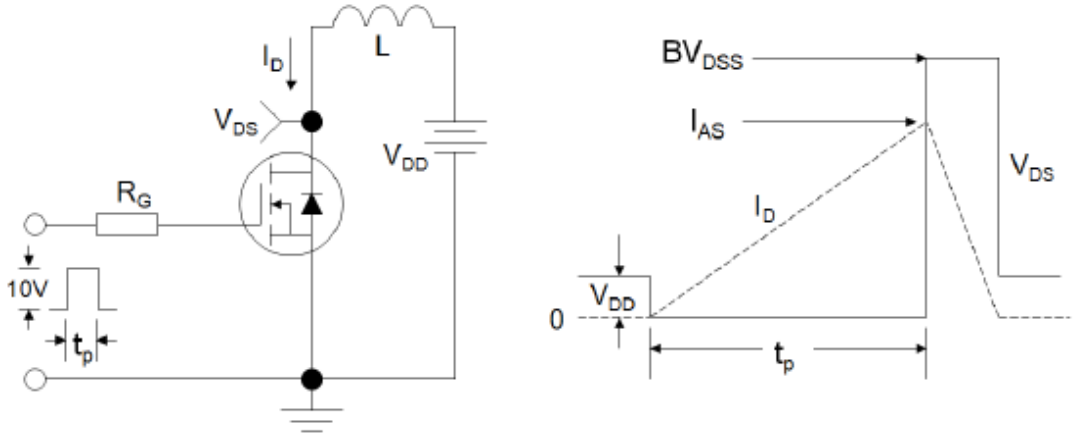



**Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms**

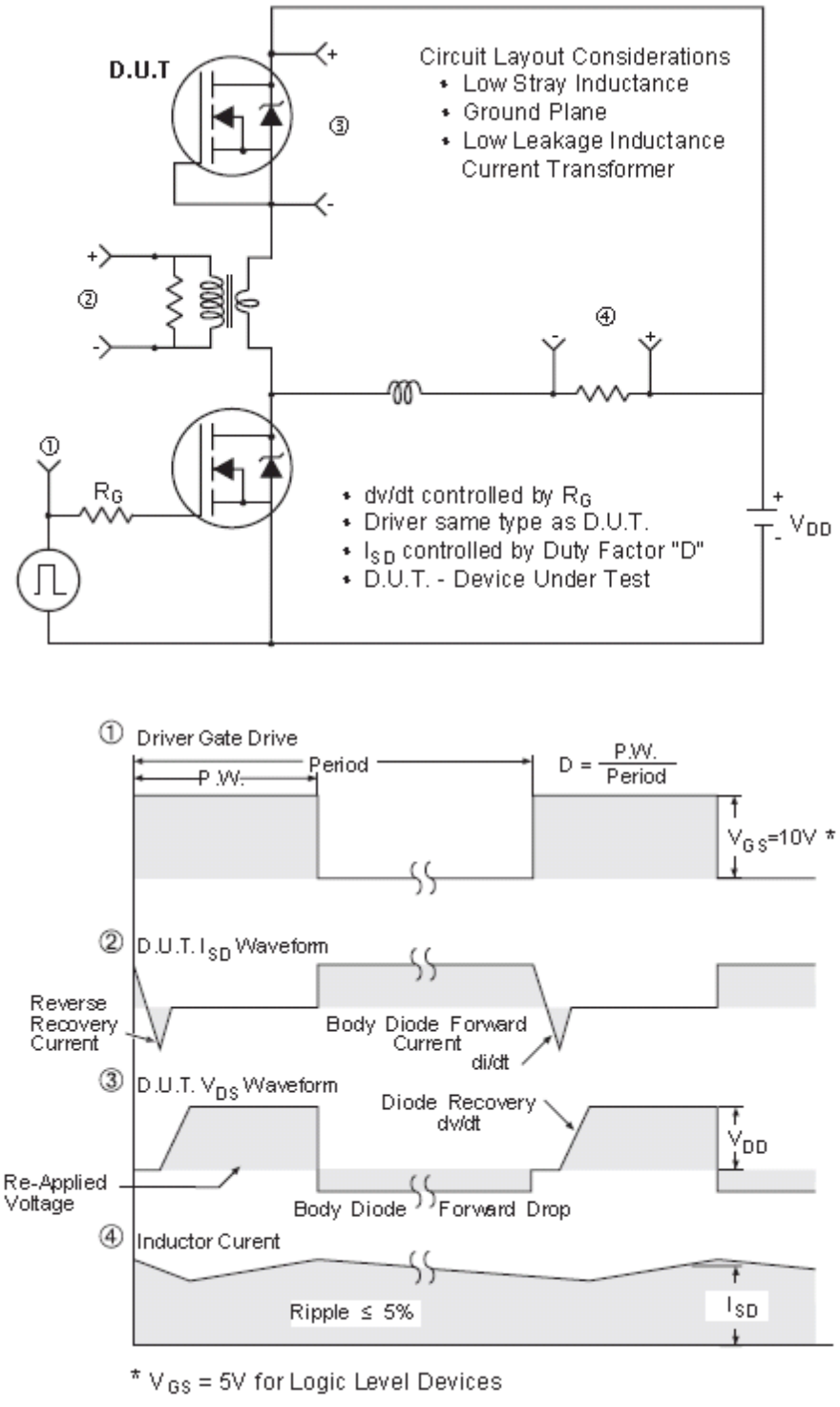



**Figure 4:Peak Diode Recovery dv/dt Test Circuit & Waveforms (For N-channel)**

## 72 3DFNDJH,QIRUPDWLRQ

| 6\PERO | ' LPHQVLRQV,Q0 LOOLPHWHUV | | ' LPHQVLRQV,Q,QFKHV | |
|---|---|---|---|---|
| | 0LQ | 0D[ | 0LQ | 0D[ |
| $ | | | | |
| $ | | | | |
| E | | | | |
| F | | | | |
| ' | | | | |
| ' | | | | |
| ' | 7<3 | | 7<3 | |
| ( | | | | |
| H | | | | |
| / | | | | |
| / | 7<3 | | 7<3 | |
| / | | | | |
| / | 7<3 | | 7<3 | |
| / | | | | |
| - | | | | |
| | e | e | e | e |
| K | | | | |
| 9 | 7<3 | | 7<3 | |